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STUDY ON STRUCTURAL AND DIELECTRIC PROPERTIES OF Sr DOPED $PbTiO_3$ FERROELECTRIC MATERIALS

Yee Yee Oo[1], War War Thin[2]

Abstract

We used spin coating to fabricate a Sr doped $PbTiO_3$ thin film on n-Si subtract. By means of X-ray diffraction and scanning electron microscopy analyses, it was confirmed that tetragonal structure at an as-synthesized state. The variations of capacitance (C) with frequency at different temperatures were also observed. It was found that the capacitance was frequency dependent at all temperatures but almost independent in the high frequency range beyond 3 kHz. From the variation of dielectric loss (tanδ) with frequency it was seen that tanδ values increase rapidly with frequency and attains a minimum value. Reverse C-V characteristics exhibited a linear $1/C^2$ versus V plot, from which a built-in potential of 0.71 V-0.85 V were deduced.

Keywords: Sr doped $PbTiO_3$ thin film, X-ray diffraction, scanning electron microscopy, Reverse C-V characteristics

Introduction

Ferroelectric thin films have been developed widely in recent years due to their potential applications including infrared detectors, actuators, and nonvolatile memories etc. Among the ferroelectric materials, lead titanate family such as $PbTiO_3$, $PbZrTiO_3$, $PbLaTiO_3$ . . . . are desirable for these applications due to the high dielectric constant, and large remnant polarization (Pontes.F.M et al, 2004). They have large spontaneous polarization and the ability to switch polarization direction. Ferroelectrics with perovskite structure (ABO_3), such as barium titanate and lead titanate are the most popular oxides because of their great properties for use in thin film capacitors, electronic transducers, actuators, high-k dielectrics, pyroelectric sensors, and nonlinear optics (Jun Wang et al, 2010). A perovskite solid solution of $PbTiO_3$ and $SrTiO_3$ (PST) exhibits the high dielectric constant of $PbTiO_3$ and the lattice stability of $SrTiO_3$ (Kyoung-Tae Kim at al, 2002).

$PbTiO_3$ reaches ferroelectric at room temperature and its Curie point is found to be at $490^{o}C$,as reported first by Shirane et al. and independently, by Smolenskii.

The structure of $PbTiO_3$, at room temperature, involves a tetragonal distortion from the pervosktite lattice, and its compound is amorphous with tetragonal (Ming-Chi Hsu et al, 2006). Nanosized PST powders have also been receiving great interest due to their novel physiocochemical properties (S. Sriram, M et al, 2009).

In this work, growth mechanism of Sr (6mol%) doped $PbTiO_3$ thin film devices is presented. Structural and microstructural properties, frequency dependent of dielectric properties, reverse C-V characteristics of the thin film devices are investigated.

Experimental Details

Sample Preparation

The raw materials of PbO, TiO_2 and $Sr(NO_3)_2$ are first weighed according to the stoichiometric formula. These powder materials are mixed to form $Pb_{1-x}Sr_xTiO_3$ with x= 0.06

[1.] Dr, Associate Professor, Department of Engineering Physics, Technological University (Maubin)
[2.] Department of Physics, West Yangon University

molar ratio. The mixture powder is ground by agate mortar to obtain the homogeneity and the primary heat treatment at 750^{o}C for 1 hr. After that the crystalline powder is ground by agate mortar for second time in the same way as before. This sample is heat treated at 750^{o}C for 1hr.

2-metoxyethanol ($CH_3OCH_2CH_2OH$) is added to the powder and then stirred and heated in a vessel with water-bath at 100°C for 1hr. The homogeneous precursor solution is obtained and ready to deposit into substrates. Before deposition, Si substrates are cleaned with standard semiconductor cleaning process. The Si substrate with dimension (1cm x1cm) are used as substrate and washed with dilute HF: DW (1:5) to remove native oxide and dry at room temperature. They are immersed in acetone for 5 minutes and dry at room temperature. After that, the precursor solution is deposited on Si substrates by spin coating technique. Later, layers are first dried at room temperature and annealed at 500°C, 550°C, 600°C, 650°C, and 700°C, respectively by conventional annealing process. Deposition procedures are carried out in the clean chamber. Finally, $Pb(Sr)TiO_3$, PST thin films are obtained. Crystallographic investigation of the films is examined. Microstructural properties of films are determined. Dielectric properties and reverse C-V characteristics of the thin film devices are investigated.

Results and Discussion

Structural Characterization

The x-ray diffraction is a convenient method to identify an unknown sample by determining its crystal structure and comparing it with a repository of standard powder diffraction patterns. XRD is performed using monochromatic Cu K_α radiation (λ=1.54056 Å) operated at 40kV (tube voltage) and 20mA (tube current). Sample is scanned from 10° to70° in diffraction angle, 2θ with a step-size of 0.02°. The XRD profiles are recorded and shown in Fig. 1(a-e). There are 14 peaks on pattern of all films and agree with the typical $PbTiO_3$ pattern of single phase perovskite structure. From the profile, it is clear that all XRD images are not remarkably different in variation nature. It is obvious that, all XRD profiles show no preferred orientation and polycrystalline. The intensity of (101) reflection is much stronger than that of remaining 13 $PbTiO_3$ peaks. It means dopant Sr ions are partially occupied into Pb-site in $PbTiO_3$ structure.

The (001) peak is occurred as first refraction of XRD spectra in all films. It is found that, all XRD profile shows pure $PbTiO_3$ structure. As the a-axis, (100) is formed as 2nd peak on XRD profile for all fabricated sample. Temperature dependence of a-axis, c-axis and c/a are evaluated and collected in table 1. Ions of alkali-earth metals, Sr^{2+} which has ionic radius 1.27 Å is frequently used to substituted Pb^{2+} (with an ionic radius of 1.32Å). Using element substitution, one can change properties of the piezoelectric ceramic, but still maintain its perovskite structure.

The width of the peaks in a particular phase pattern provides an indication of the average crystallite size. Large crystallite gives rise to sharp peak, while the peak width increase as crystallite size reduced. The average grain size, G is also estimated from the half-width of the x-ray diffraction peaks. Peak broading also occurs as results of radiations in d-spacing caused by micro-strain. However, the relationship between broading and diffraction angle, 2θ is different from that of crystallite size effects making it possible to differentiate between the two phenomena. The FWHM values of dominant reflections are found to be 0.00942, 0.00748, 0.00536, 0.00489 and 0.00359 for respective specimens. As it is shown in table, it is significantly obvious that the crystallite size variation is inversely changed compared to that of FWHM. These values were collected and listed in table 2.

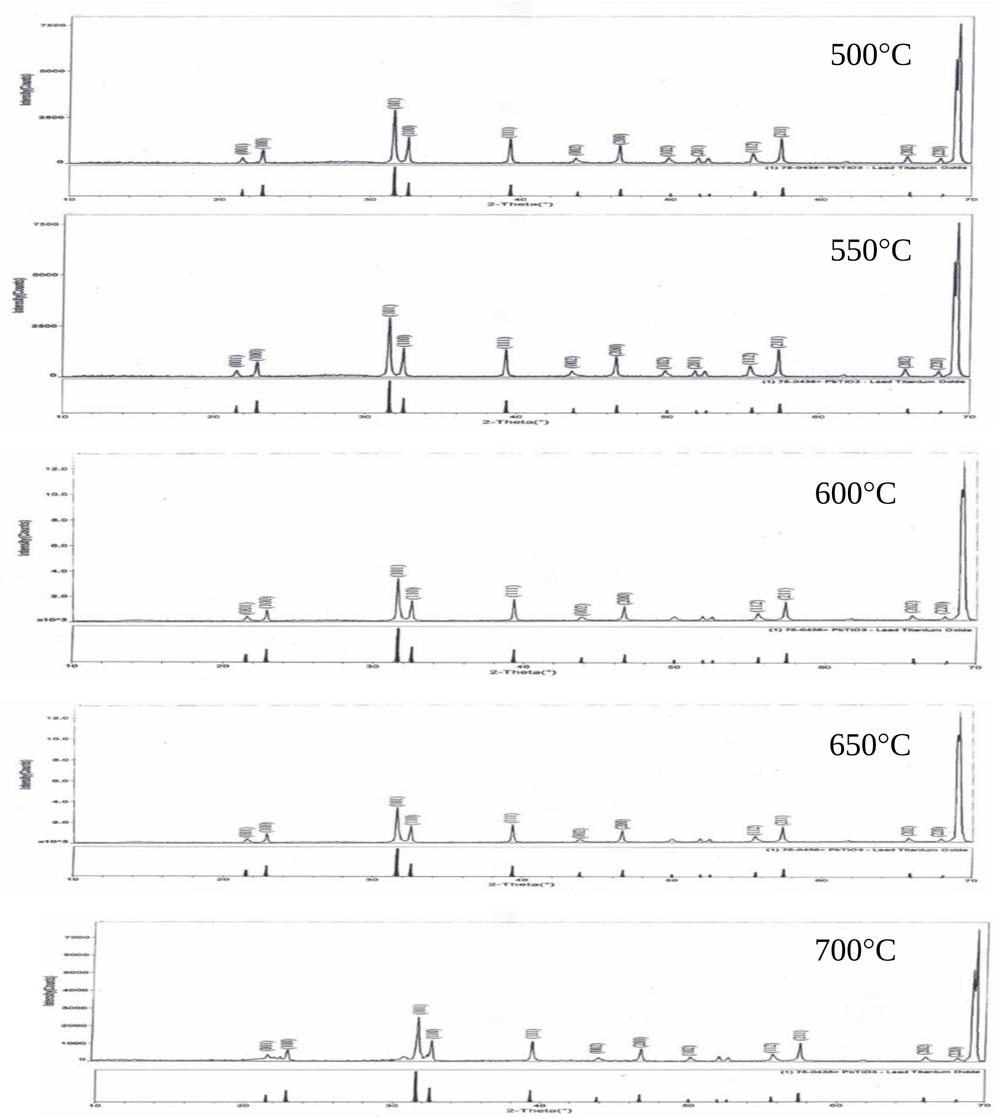

Figure 1 XRD patterns of Pb(Sr)TiO_3 TFD at process temperature (a) 500^{o}C (b) 550^{o}C (c) 600^{o}C (d) 650^{o}C (e) 700^{o}C

Table 1 Temperature dependence of lattice parameters (a and c) and c/a

Temperature(^{0}C)	a (Å)	c (Å)	c/a
500	3.9870	4.1284	1.0354
550	3.7982	4.1436	1.0909
600	3.9872	4.1339	1.0367
650	3.9971	4.1289	1.0329
700	3.7850	4.1304	1.0912

Table 2 FWHM and crystallite size of all fabricated sample

Temperature(^{0}C)	FWHM(deg)	crystallite size(nm)
500	0.00942	93.77
550	0.00748	147.15
600	0.00536	179.22
650	0.00489	213.47
700	0.00359	235.99

Microstructural Characterization

SEM investigation of Sr (6 mol %) doped $PbTiO_3$ films annealed at changing the process temperatures are shown in Fig. 2(a - e). The surface of the films became fairly dense after annealing at process temperatures from 500ºC to 700ºC. Fig. 2(a) shows bubble like morphology is observed in Sr (6 mol%) doped PST thin film device at process temperature 500ºC. The grain sizes are not uniform but also crack free. The grain size is found to 3.953 µm. Fig. 2 (b) shows the SEM photograph of Sr (6mol %) doped PST thin film device at process temperature 550ºC. From this Fig., it is clear that the grain sizes of this film are not uniform but crack free. The grain size is found to be 3.66 µm. From the Fig. 2 (c - e), it is obvious that, grain sizes are not uniform, crack free and no pin- hole arrangement.

Grain sizes of Sr (6 mol %) doped PST thin film devices at various process temperatures are listed in table 3. The increase of pore and grain-growth are observed with the increase of process temperature from 550ºC to 650ºC. The maximum grain size is at process temperature 650ºC. It is observed that the grain-size varies with process temperatures.

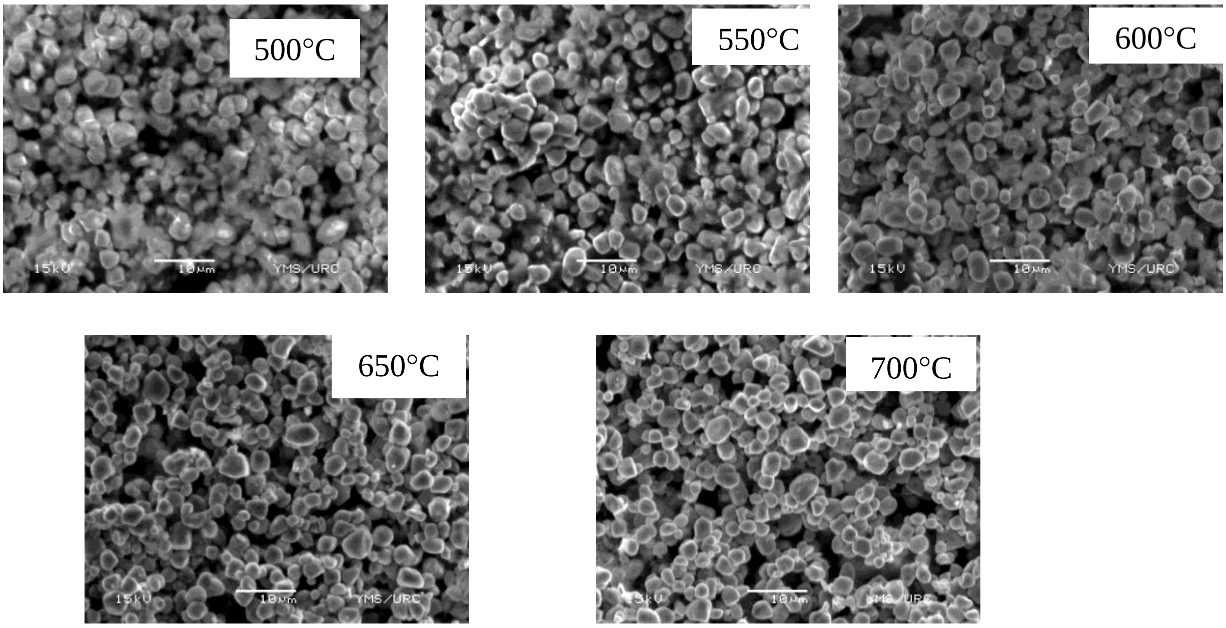

Figure 2 SEM photograph of PST thin film device at process temperature (a) 500^{o}C (b) 550^{o}C (c) 600^{o}C (d) 650^{o}C (e) 700^{o}C

Table 3 Average grain size of $Pb(Sr)TiO_3$:Si thin film devices

Temperature (^{o}C)	Grain size (µm)
500	3.953
550	3.666
600	3.820
650	4.353
700	4.313

$1/C^2$ – V Characterization

C-V measurements are performed in the region of -4 V to +4 V at 100 kHz frequency. From this measurement, $1/C^2$ – V characteristics of these films are also studied.

A plot of $1/C^2$ as a function of V is a straight line whose intercept on the voltage axis gives V_{bi} and the slope can be used to determine the effective dopant concentration N_i. Fig.3 (a-e) display $1/C^2$-V characteristics of Pb(Sr)TiO_3:Si thin film devices at process temperature 500°C, 550°C, 600°C, 650°C and 700°C, respectively. The results of the $1/C^2$ -V characteristics of Pb(Sr)TiO_3:Si thin film devices at room temperature measured at frequency of 100 kHz. The value of the built-in voltage, dopant concentration and depletion layer width have been calculated and described in Table 4. The values of V_{bi} is the highest at process temperature 600°C and the lowest at process temperature 700°C. The measurement of N_I is the highest at process temperature 500°C and the lowest at process temperature 650°C. Depletion layer width (W) is increase with increasing process temperature. So, W is the highest at process temperature 700°C and is the lowest at process temperature 500°C.

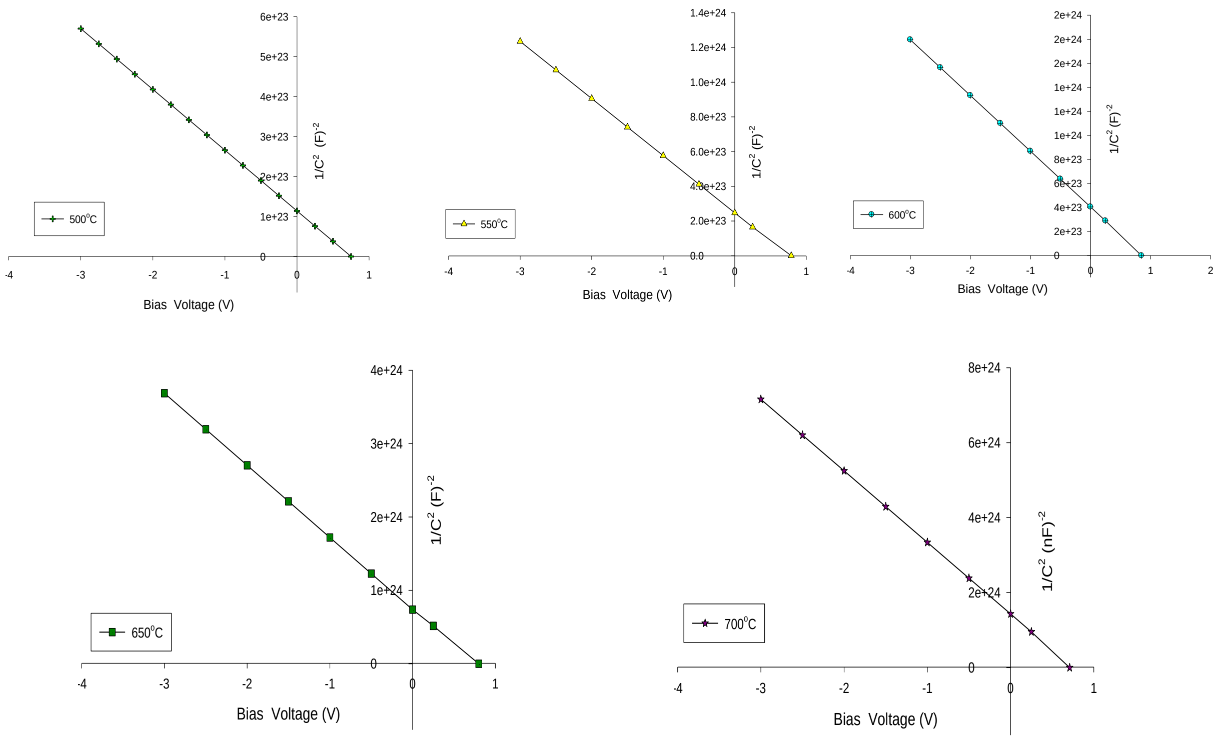

Figure 3 $1/C^2$-V characteristic of Pb(Sr)TiO_3:Si thin film devices at process temperature 500°C (b) 550°C (c) 600°C (d) 650°C (e) 700°C

Table 4 Built-in voltage, dopant concentration and depletion layer width of $Pb(Sr)TiO_3$:Si thin film devices

Process Temperature (°C)	V_{bi}(V)	N_i (cm^{-3})	W (cm)
500	0.75	7.83×10^{15}	7.92×10^{-5}
550	0.79	3.64×10^{15}	1.16×10^{-4}
600	0.85	2.56×10^{15}	1.40×10^{-4}
650	0.80	1.12×10^{15}	2.01×10^{-4}
700	0.71	6.2×10^{15}	2.80×10^{-4}

Dielectric Properties Characterization

The AC parameter such as capacitance "C" and dissipation factor "D" are measured using LCR meter (Quad Tech, 1730 digibridge) and Cu electrode in the frequency range 1kHz to 100kHz at zero bias.

Frequency dependence of capacitance of $Pb(Sr)TiO_3$:Si thin film devices (TFDs) at various process temperatures is depicted in Fig. 4. Measurements are performed at zero bias. From this figure, it is obvious that capacitance decreases with increasing frequency. It is due to "RC" time effect. Capacitance versus ln f characteristic measurement of this devices at various process temperature is described in Fig. 5. From this figure, the value of capacitance decreases with increasing frequency.

Dielectric constant (ε_r) versus ln f characteristic measurement of $Pb(Sr)TiO_3$:Si TFDs at various process temperature is demonstrated in Fig. 6. From this characteristics, ε_r decreases with increasing frequency. Dielectric loss ($\tan\delta$) is the ratio of imaginary part of the dielectric constant to the real part of the dielectric constant. The frequency dependence of $\tan\delta$ at various process temperatures is depicted in Fig. 7. From the figure, $\tan\delta$ increases with increasing frequency.

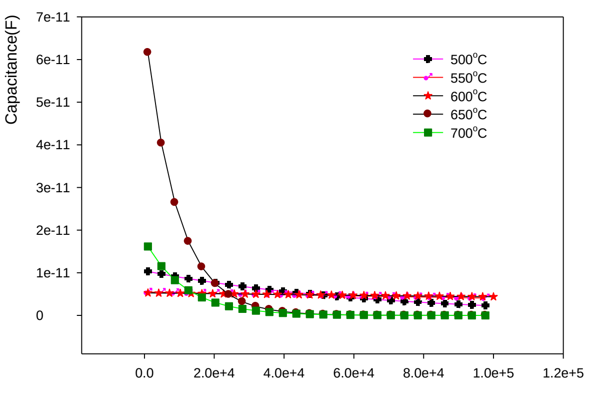

Figure 4 Capacitance - Frequency characteristic of $Pb(Sr)TiO_3$:Si thin film devices

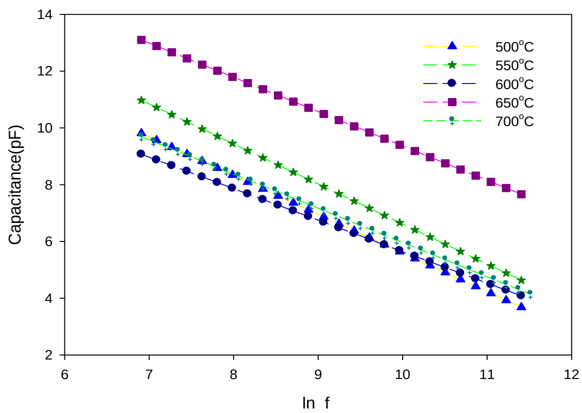

Figure 5 C-ln f characteristic of Pb(Sr) TiO_3:Si thin film devices

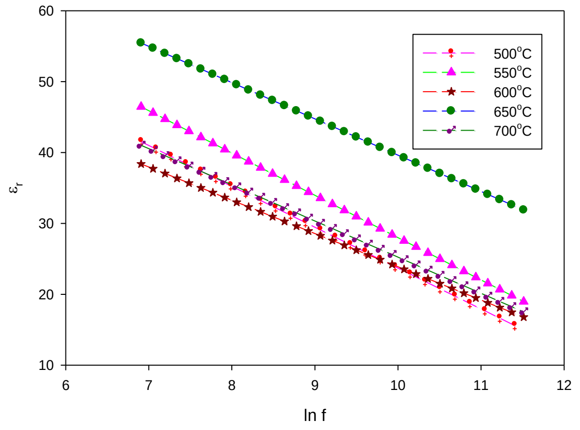

Figure 6 ε_r - ln f characteristic of $Pb(Sr)TiO_3$:Si thin film devices

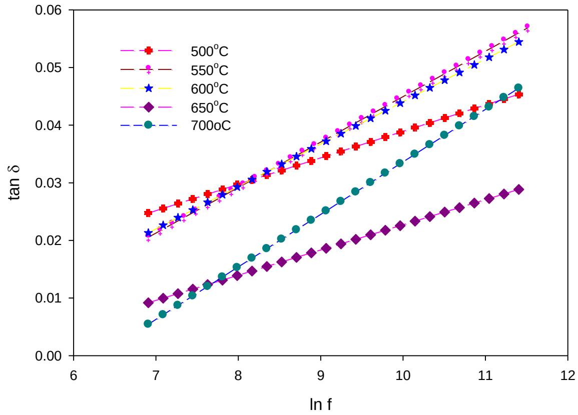

Figure 7 tan δ–lnf characteristic of $Pb(Sr)TiO_3$:Si thin film devices

Conclusion

Preparation and characterization of Sr doped lead titanate thin film devices have been investigated. In XRD profiles of $Pb(Sr)TiO_3$, there are 14 peaks on pattern of all films and agree with the typical $PbTiO_3$ pattern of single phase perovskite structure. And, it is clear that all XRD images are not remarkably different in peak formation. All XRD profiles show no preferred orientation and polycrystalline. Using element substitution, one can change properties of the piezoelectric ceramic, but still maintain its perovskite structure. SEM investigation of $Pb(Sr)TiO_3$ TFDs are annealed at changing the process temperatures had been studied. The increase of pore and grain-growth are observed with the increase of process temperature from 550ºC to 650ºC. The maximum grain size is at process temperature 650ºC. C-V characteristics of $Pb(Sr)TiO_3$:Si thin film are examined by using Cu electrode and Quad Tech LCR Digibridge meter model 1730. Measurements are performed in the region of -4 V to +4 V at 100 kHz frequency. From this measurement, $1/C^2$ – V characteristics of these films had been also studied. The value of built-in voltage V_{bi} for Si based thin films should be less than 1 V at room temperature (300 K). The V_{bi} values of $Pb(Sr)TiO_3$:Si thin film are followed the above condition. So, $Pb(Sr)TiO_3$:Si thin film are acceptable for diode application. The AC parameters such as capacitance "C" and dissipation factor "D" are measured using LCR meter (Quad Tech, 1730 digibridge) and Cu-electrode in the frequency range 1 kHz to 100 kHz at zero bias. The variations of dielectric constant and dielectric loss of ceramic had been investigated. It is found that, RC time effect is observed in frequency dependence of the dielectric constant characteristics.

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